

# How To Design the Perfect PCB Stack Up With Altium Designer

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In the last 20+ years, electronics have become increasingly more complex. Board density was pushed to the limits. EMC/EMI regulations evolved and got stricter. Speeding edges got smaller. Therefore, the PCB Layout engineer needs a good understanding of EMC, PDN, EMI, and SI in order to route a modern PCB with confidence. In this article we'll talk about some of the considerations we should have in order to create a PCB stack up correctly.

## What Are We Going to Learn?

In this article, we will learn how to plan a PCB stackup and then how to implement it in Altium. We will consider some design optimization to minimize the SI issue when we have an HSD (High speed digital design.)

### We will learn

- How to understand the datasheet of PCB laminate materials.
- How to estimate the number of signal layers.
- Some suggestions on how to design the PCB stackup with Altium.
- Typical mistakes and pitfalls, and how to use Altium to avoid them.

## Understanding The PCB Laminate Material Datasheet

The first step a PCB Layout engineer should do is to select the PCB laminate materials (resin, copper foil, weave of the glass) for his/her application. The choice of PCB laminate depends on the type of application.

For example:

- HSD (High speed digital circuit), typical applications are servers, router, high speed data channels (e.g. PCIe, 10Gbe, etc.). Requires laminate like FR408HR, I-speed, etc.
- High Thermal reliability, typical applications are Automotive, Aerospace, Military. Requires laminate like P95/P25 (with high Tg/Td).
- RF & microwave. Requires laminates like IS680 TerraGreen(RF/MW) , etc.
- Halogen-free, typical applications are Transportation, mobile and wireless devices. Requires laminate like TerraGreen.
- HDI (High Density Interconnect), typical applications are Layer count reduction, Military and Aerospace. Requires laminate like I-Speed, FR408HR, etc.
- Polyimide, typical applications are Military, Aerospace, Requires laminate like P25N, P95/P25, etc.

In order to select the right material, we need to understand the PCB datasheet.

## **Key Parameters To Watch For**

### **CTE**

The coefficient of thermal expansion (CTE) expressed in PPM. Usually, it is higher on the z axis than on the x and y axes. This parameter is critical on the z axis. When it is too high during assembly, we may have micro-cracks on vias from the different expansions between the laminate and copper.

Instead, The CTE-x,y is a parameter to watch when designing electronics with a lot of thermal cycles. For example in the aerospace industry, the CTE-x,y is very important since LEO satellites have orbit periods of 90-120 minutes, exposing the satellites to a large number of thermal cycles, which may cause cracks on the component sides.

### **Tg, Glass Transition Temperature**

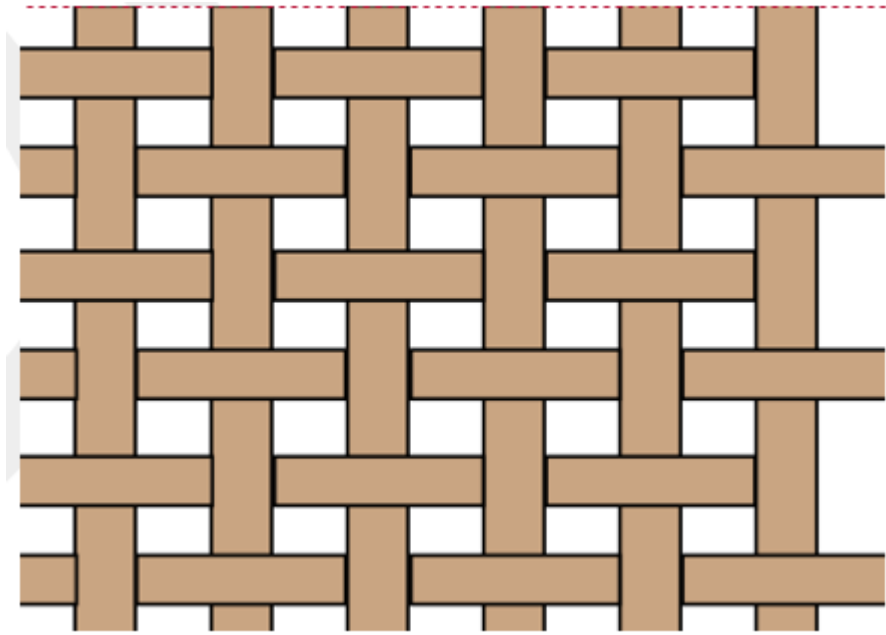
The Tg is the temperature at which the prepreg resin transits from rigid to reasonably elastic material (i.e melts).

### **Td, Decomposition Temperature**

As the name suggests, this is the temperature where the prepreg material decomposes and starts to lose its properties.

### **Dk, Dielectric Constant**

This parameter is the average dielectric constant for the core and prepreg materials. I'm using the word average because if we are looking at the structure of a prepreg weave of glass it will look like:



*Figure. 1 prepreg fibre pattern example*

Figure 1 prepreg: The resin will fill the gaps of the glass structure, creating a dielectric Dk1 zone and one with Dk2. At very high frequencies, this may cause some issues (not discussed in this article). The key point is that, when designing HSD circuits, you need to select a prepreg that is as homogenous as possible, like I-Speed, FR408HR, Tachyon 100G.

## **Tan( $\delta$ ) Or Df, Loss Tangent Or Dissipation Factor**

An electromagnetic waveform traveling through a dielectric material is partially absorbed by the material. This absorption is measured by a parameter usually referred as Dk in the datasheet. It translates into an attenuation per inch using the eq.1:

$$Att=2.3 f \tan(\delta) \sqrt{\epsilon_r} \text{ (dB/in)} \text{ [eq. 1]}$$

Where f = frequency in GHz, and  $\epsilon_r$  is the dielectric constant of the material

Example: The Isola FR408HR has  $\epsilon_r = 3.7$  and  $\tan(\delta) = 0.011$  therefore at 10 GHz has an attenuation of  $Att(10\text{GHz}) = -0.94$  (dB/in). So, using FR408HR after just 3 inches we have lost already -3 dB.

## **How Estimate The Number Of Signal Layers**

In order to design the PCB stackup, we need to guess the number of layers we need.

There are two interesting ways to do this.

- The first way [1] assumes the components with the highest number of pins, e.g. a BGA component, dictates the worst-case scenario. Using this method, you estimate the number of signal layers by taking the number of IO pins rows (or columns), divide the number by 2, and then round up the result to the nearest even number. E.g. if a BGA has an IO rows (columns) deep of 11, then a good guess for the minimum number of IO layers is 6.

- The second way is using Rent's rule.[2] Rent was an IBM engineer who popularized the way he estimated the average trace pitch. According to the rule, if you have M routing layers and N interconnections [2], the average pitch, in inches, is equal to:

$$P_{avg} = (XY)^{1/2} / N \quad [eq. 2]$$

Where X and Y are the board's X and Y dimension in inches. Therefore, you can estimate the number of routing layers by estimating M, and then seeing if the resulting pitch is compatible with the PCB technology.

## Reference Plane Considerations

After estimating the number of routing layers, we must decide the number of planes.

- The 0V plane gives a return path to high speed signals (always route a critical trace within 2 planes). Therefore, you must ensure the 0V plane extends as far as possible.
- All planes resonate! Every plane works as an antenna and will resonate at [3]

$$F_{GHz} = 150 \sqrt{(l/L)^2 + (m/W)^2} \quad [eq. 3]$$

Where l and m are the modes, and W and L are the dimension in mm. For example, if a plane has the dimension of 100mm x 50mm, then the first mode should resonate around 1.34 GHz. Why do we need this information? Because during the EMC testing (Radiated Emission), if we find a peak around 1.34 GHz, which is not a multiple (or intermodulation) of any clocks, then you know that your plane is probably resonating. (There are design techniques to increase the resonance frequency, but they are out of the scope of this article).

- Cavity resonance between planes. To prevent cavity resonance between 2 planes at same potential (e.g. 0V), stick the planes vias at a distance no more than  $\lambda / (10 \sqrt{\epsilon_r})$  [3].
- Reduce the Q of VDD-GND plane. Every VDD-GND plane serves an important rule. It distributes capacitance while it resonates. If it has a high capacitance, it will most likely fail the Radiated Emission. One way to avoid this is to put the 2 planes as close together as possible (increasing the C and reducing the Q).

## Planning PCB Stackup with Altium

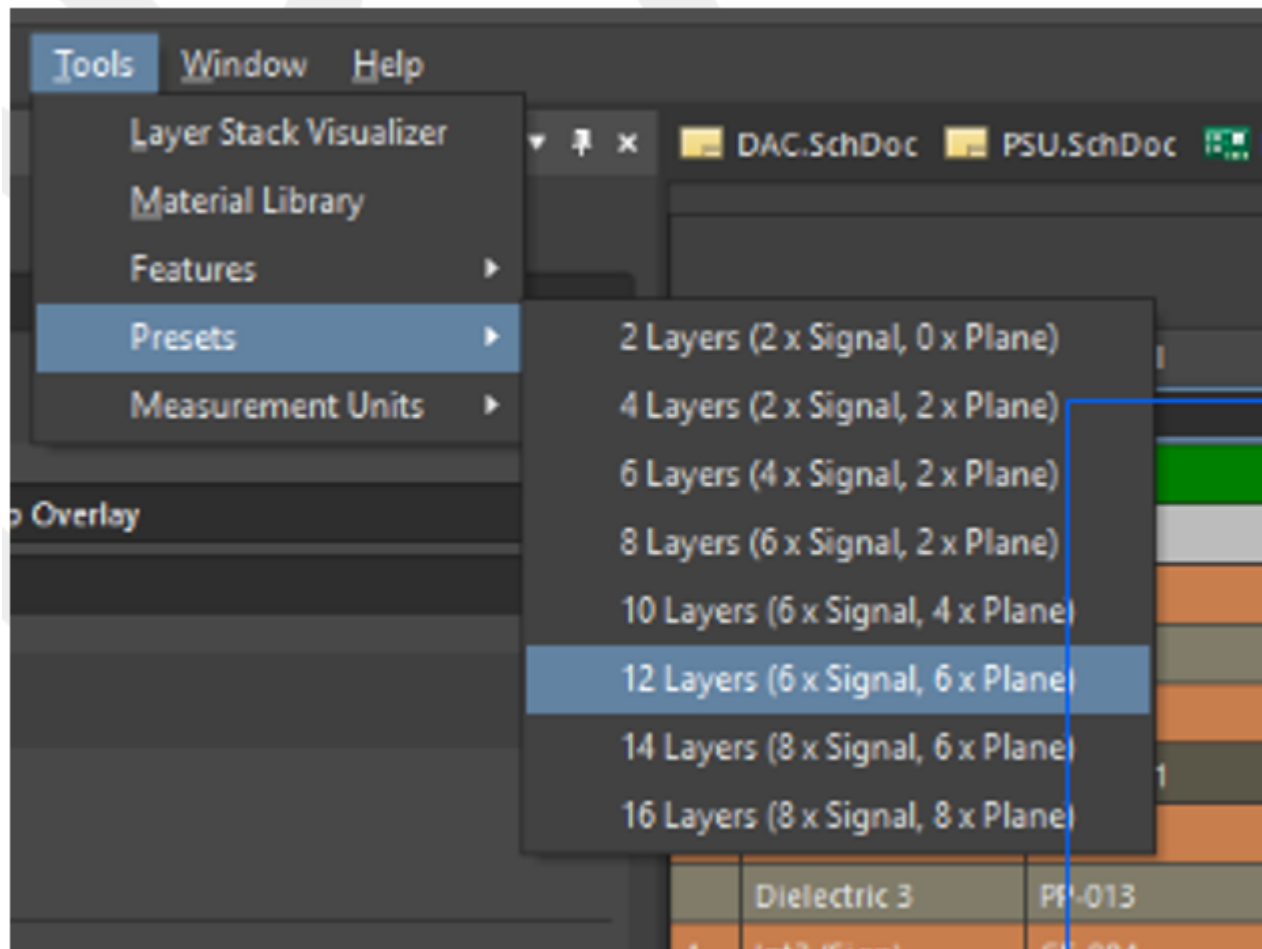
It is now time to design the PCB stackup. From what we wrote above, we already have the following:

1. Number of signal layers
2. Minimum number of Plane
3. Critical signal (clock, ddr, USB)
4. PCB laminate material

From point 1 and 2, we have a good idea of the number of layers your application needs. Let us say we have about 6 layers for the signals and 6 layers for the plane. We can start Altium to save time! Open your PCB project and create a PCB document.

Then select the Layer Stack Manager; from here select

Tool->Presets and Select 12 Layers.



Altium will create the default PCB stackup that should look like:

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	SM-001	Solder Mask		0.025mm	4	0.03
	Top Copper Plat...	PbSn	Copper plating		0.02mm		
1	Top Layer	CF-004	Signal	1oz	0.035mm		
	Dielectric 1	PP-013	Prepreg		0.097mm	4.3	0.02
2	Int1 (GND)	CF-004	Plane	1oz	0.035mm		
	Dielectric 2	Core-011	Core		0.102mm	4.4	0.02
3	Int2 (PWR)	CF-004	Plane	1oz	0.035mm		
	Dielectric 3	PP-013	Prepreg		0.097mm	4.3	0.02
4	Int3 (Sign)	CF-004	Signal	1oz	0.035mm		
	Dielectric 4	Core-011	Core		0.102mm	4.4	0.02
5	Int4 (Sign)	CF-004	Signal	1oz	0.035mm		
	Dielectric 5	PP-014	Prepreg		0.107mm	4.2	0.02
6	Int5 (GND)	CF-004	Plane	1oz	0.035mm		
	Dielectric 6	Core-011	Core		0.102mm	4.4	0.02
7	Int6 (PWR)	CF-004	Plane	1oz	0.035mm		
	Dielectric 7	PP-014	Prepreg		0.107mm	4.2	0.02
8	Int7 (Sign)	CF-004	Signal	1oz	0.035mm		
	Dielectric 8	Core-011	Core		0.102mm	4.4	0.02
9	Int8 (Sign)	CF-004	Signal	1oz	0.035mm		
	Dielectric 9	PP-013	Prepreg		0.097mm	4.3	0.02
10	Int9 (GND)	CF-004	Plane	1oz	0.035mm		
	Dielectric 10	Core-011	Core		0.102mm	4.4	0.02
11	Int10 (PWR)	CF-004	Plane	1oz	0.035mm		
	Dielectric 11	PP-013	Prepreg		0.097mm	4.3	0.02
12	Bottom Layer	CF-004	Signal	1oz	0.035mm		
	Bottom Copper...	PbSn	Copper plating		0.02mm		
	Bottom Solder	SM-001	Solder Mask		0.025mm	4	0.03
	Bottom Overlay		Overlay				

We now need to modify the above stackup with the PCB laminate material we have selected for our application.

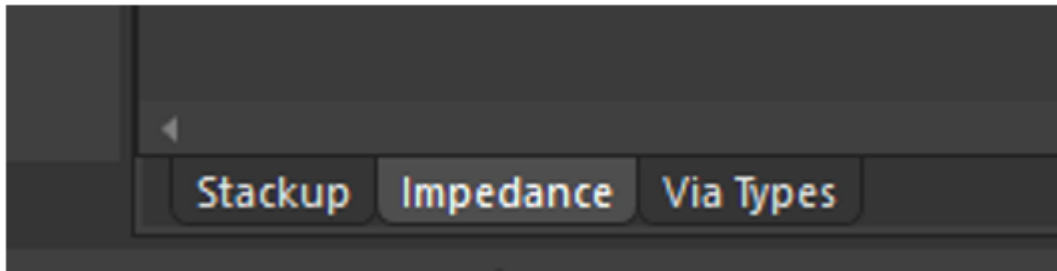
If we are not happy with the default materials, we can change them and insert the correct material, thickness, Dk, and Df.

The default stackup that comes with Altium already has a good symmetrical structure and is already a good example on how a stackup should be designed.

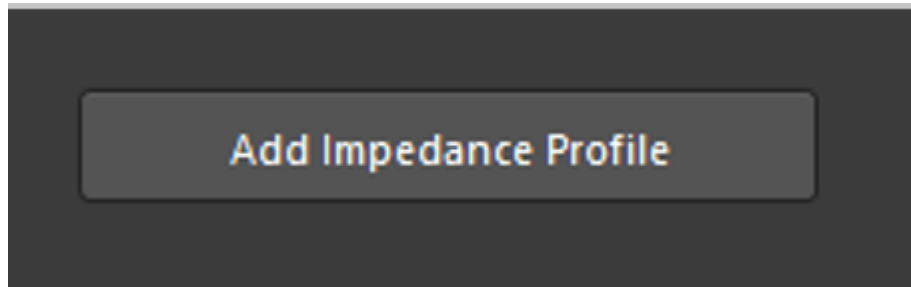
Once we are happy with the material, we must decide which layers to use for signal, critical signals, and power plane.

We should start planning the critical signals first (for example clock traces, ddr traces, etc.). For example, if we have a board with some traces and a characteristic impedances of 50 and 90 ohms, we can select which layer will route those traces, and we can use Altium for that.

Click on the impedance Tab (at the bottom)



And then click on Add Impedance Profile:

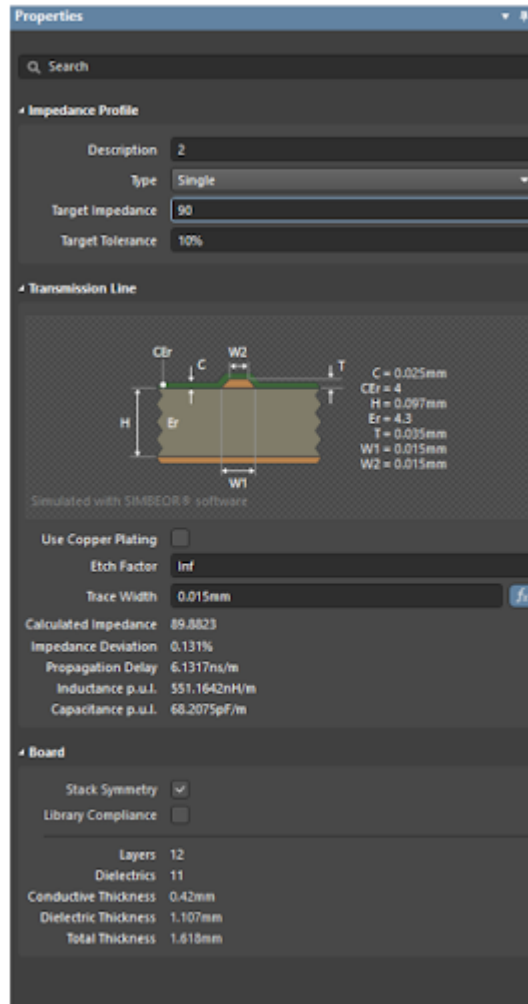


You should see the default impedance profile for a 50 ohm trace:

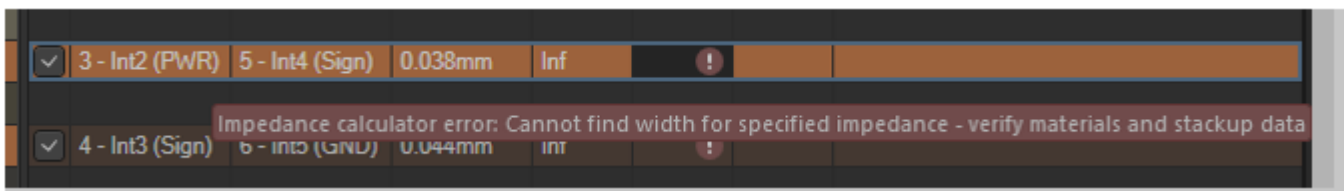
	Top Ref	Bottom Ref	Width	Etch	Z	Z Deviation	Tp
<input checked="" type="checkbox"/>		2 - Int1 (GND)	0.14mm	Inf	49.9959	0.008%	6.2197...
<input checked="" type="checkbox"/>	3 - Int2 (PWR)	5 - Int4 (Sign)	0.038mm	Inf	49.9962	0.008%	6.969n...
<input checked="" type="checkbox"/>	4 - Int3 (Sign)	6 - Int5 (GND)	0.044mm	Inf	49.9967	0.007%	6.895n...
<input checked="" type="checkbox"/>	7 - Int6 (PWR)	9 - Int8 (Sign)	0.044mm	Inf	49.9967	0.007%	6.895n...
<input checked="" type="checkbox"/>	8 - Int7 (Sign)	10 - Int9 (GND)	0.038mm	Inf	49.9962	0.008%	6.969n...
<input checked="" type="checkbox"/>	11 - Int10 (P_		0.14mm	Inf	49.9959	0.008%	6.2197...

For example, according to the above impedance profile, the width of a 50 ohm trace is around 0.14 mm at the top and bottom layers, while only 0.038 mm in the inner layers. If we are happy with this, we can go ahead, otherwise we need to change either the prepreg thickness or the laminate material.

Now, let us route the 90 ohm trace (usually for USB) by just clicking the + icon, creating a new profile, and then changing the target impedance to 90 in the property.



If a layer cannot have an impedance of 90 ohms, Altium will notify you by adding a warning to the impedance profile.



You can then change the material and repeat the above steps until you have a satisfactory solution for your requirements.

In the next article, we will see how to use Altium to avoid some of the design pitfalls when routing critical signals on a multilayer PCB.

Now you can download a free trial of Altium Designer and learn more about the stackup and impedance features. Talk to an Altium expert today to learn more.