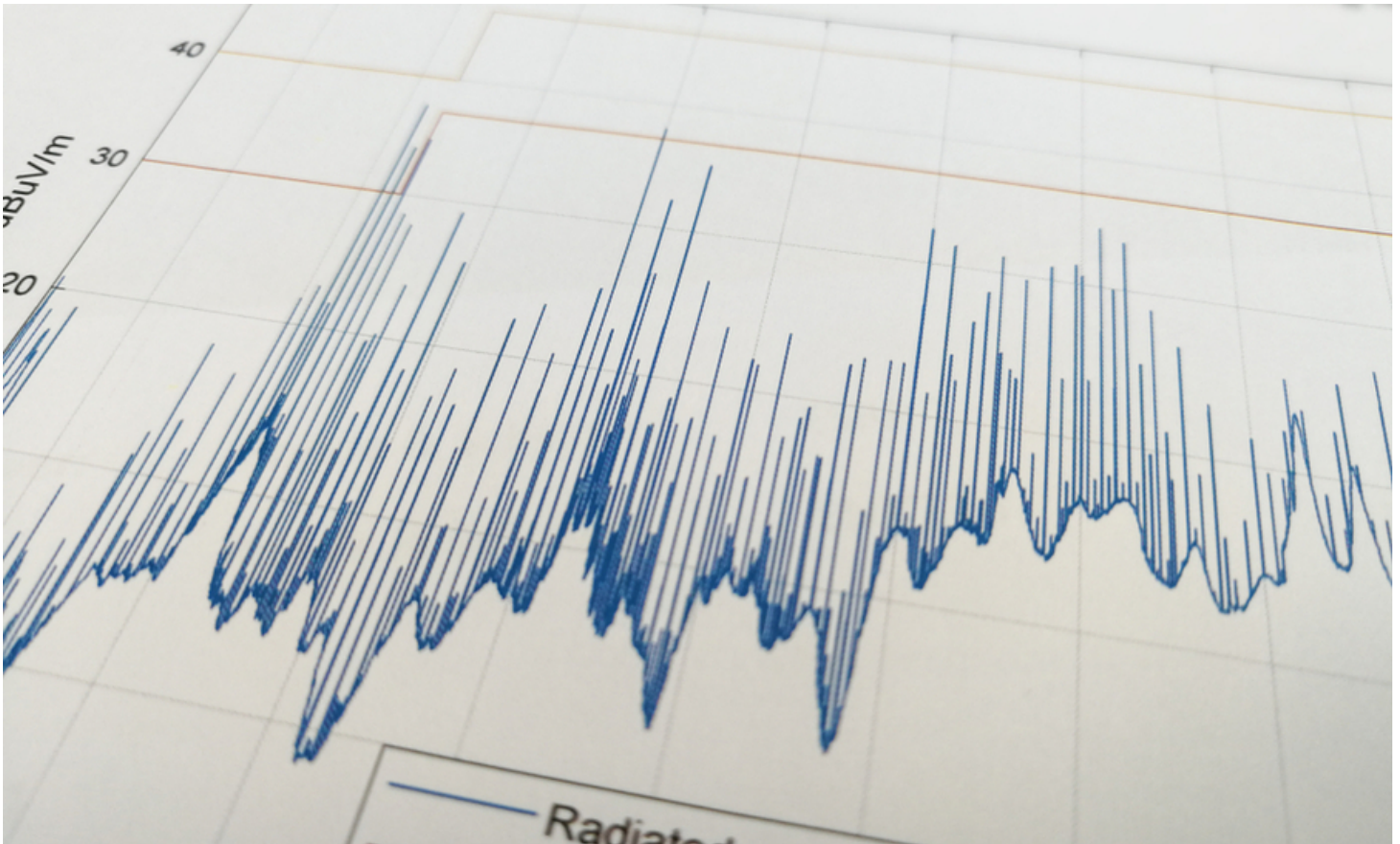


# Radiated EMI Sources in High Speed/High Frequency PCBs



Zachariah Peterson | November 17, 2019



*Radiated EMI measurements during EMC testing*

The image above shows a snapshot of results from an EMC test under CISPR requirements. This product is right at the edge of Class B limits on radiated emissions. We can see a very complicated resonance spectrum in this plot with a large number of sharp peaks superimposed on wide peaks at lower level. What causes all of this radiated noise? There a number of sources that can cause this type of emission from a board. Interestingly, the board may work just fine as long as sensitive portions of the board are properly isolated; these problems aren't obvious until you look into the far field regime.

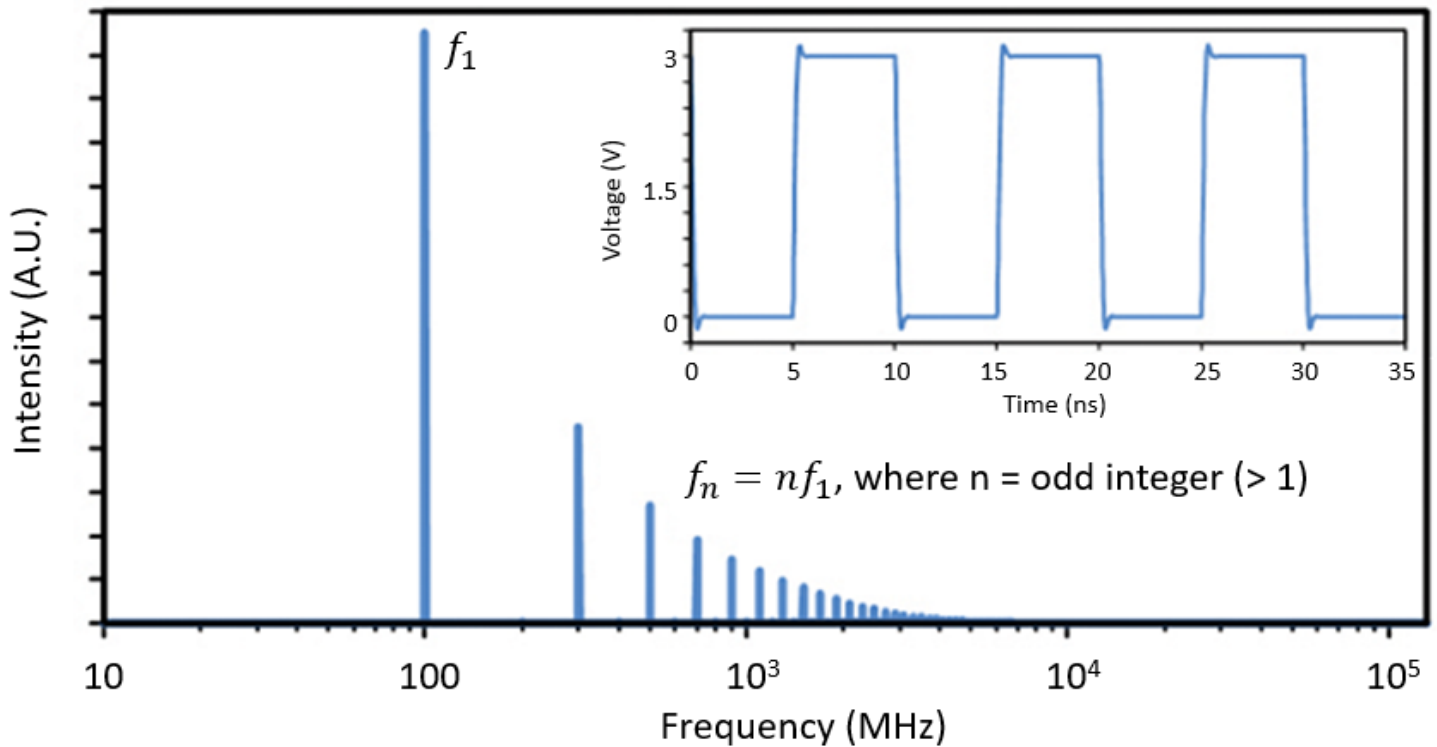
Controlling radiated EMI from trace, planes, and components requires controlling the electromagnetic field by choosing the correct geometry for your conductors and components. This means you'll need to select the right stackup for your particular operating frequency in order to control electric fields in your board. Once you move to very high frequencies (we're talking mmWave frequencies), there are other effects that can arise due to the arrangement of plane layers.

## Identifying Radiated EMI Sources from Test Results

The example test results shown above allow us to identify three sources of radiated EMI:

### Clock Harmonics

These high-Q resonances (see the very narrow peaks in the above image) are harmonics of some fundamental clock frequency. They originate from the clock signal as conducted EMI. The ideal clock signal would only contain a single frequency (the repetition rate), meaning it would be sinusoidal. Clock pulses are squared and ideally only contain odd harmonics of the fundamental frequency (again, the repetition rate). Real clock pulses also contain some even harmonic content due to non-zero rise time and/or duty cycles not equal to 50%. Finally, clock pulses, just like any digital pulse, can be inhomogeneously bandlimited due to parasitic or intentional filtering.



FFT for a stream of clock pulses (50% duty cycle). The inset shows the clock pulses in the time domain.

The electromagnetic energy in these high-Q resonances can be spread out to a broader spectral range by using spread spectrum clocking. This is normally used in PCIe and SRAM interfaces to reduce EMI, as well as in other digital systems.

## Board Resonances

When we say “board resonances,” we’re referring to a large number of electromagnetic resonances which arise due to the geometry of conductors on the board. This includes your stackup, traces, conductive elements in components, and anything else that carries an electric current. These can be low-Q resonances (the wider, lower intensity peaks in the above image) and are generally not related to each other by integer multiples of some fundamental frequency.

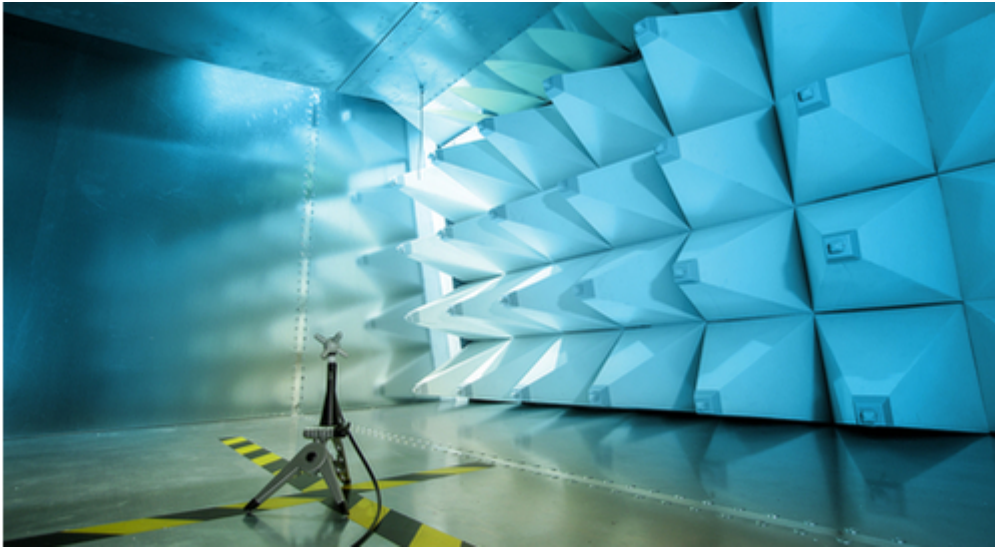
This also includes cavities in your board that provide some opportunity for the electromagnetic field to resonate in your board. This include gaps in the fiber weave in your substrate and cavities formed by parallel conductors on adjacent layers. These cavities can be lossy as they are essentially open in one or more direction, thus the frequency bands are quite broad compared to clock resonances.

Finally, if there are any unterminated transmission lines in your board, signal reflection produces standing waves with strong resonances at specific frequencies (generally even and/or odd multiples of some fundamental frequency). These also appear as high-Q resonances. These particular resonances are eliminated with proper impedance matching and impedance controlled routing.

## Transients on the Power Bus

The transient response in your power bus during switching also acts as a strong source of conducted and radiated EMI. This is analogous to what occurs in a switching regulator. As a downstream IC switches, it draws a significant amount of power through the power bus. This pulls a burst of current from the power supply and the decoupling network. This quick burst of current and the resulting transient voltage/current oscillation on the power bus acts as a source of radiated EMI. When the IC in question switches faster and draws more current, it induces a stronger pulse of radiated EMI.

The solution here is to ensure sufficient interplane capacitance and large enough decoupling capacitance to minimize the radiated power from the power bus. In other words, for a given current drawn during switching, your only solution is to minimize the voltage fluctuation by minimizing the impedance of your PDN. This is all about designing your stackup correctly. Take a look at this article from Rick Hartley in Signal Integrity Journal for some stackup recommendations to combat radiated EMI resulting from power integrity problems.



*GTEM cell for EMC testing*

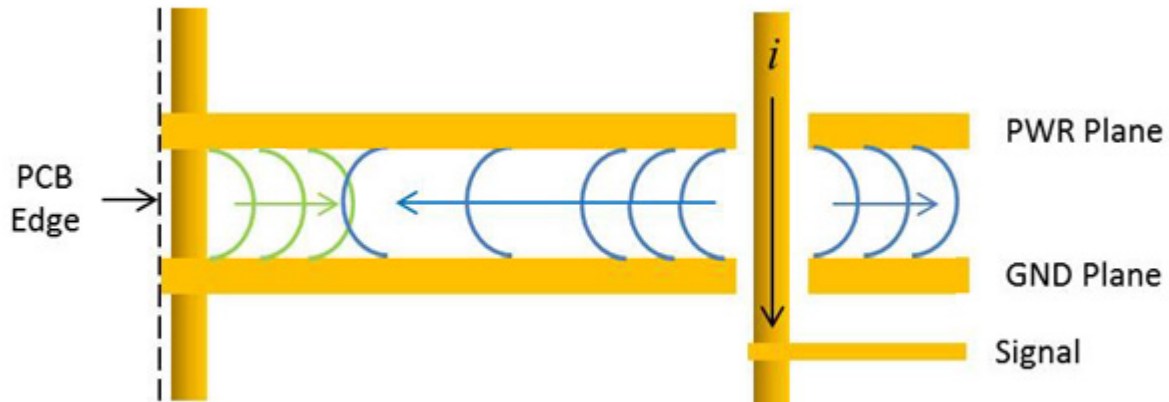
## Cavity Resonances

Cavity resonances were mentioned in the list above as a source of radiated EMI. Any AC/switching digital signal that travels along a trace produces an electromagnetic wave, which can excite cavity resonances throughout your board. These cavities do not need to be located near the trace in question; the cavities can be non-local, meaning the electromagnetic field travels away from the conductor in question and excites a resonance elsewhere in your board.

These cavities, by definition, are open cavities, meaning some field will leak out from the board as the electromagnetic field propagates. Cavities with strong resonances can be a prominent source of radiated EMI, and the strongest emission tends to be observed from the edges of your board; this is known as the cavity resonance edge effect (CREE) within the research community. One example is a case involving incorrect placement of a ground plane below a crystal oscillator, which effectively forms a center-fed patch antenna.

Routing traces close to their reference planes ensures circuits have reduced EMI susceptibility, and also ensures that a given circuit emits less radiation (thanks to reciprocity). This is because a stronger, more tightly coupled image signal is induced in the plane layer. Placing traces and planes closer together also causes the resonances corresponding to board cavity emissions. Gaps in the fiber weave can have fundamental resonances in the GHz range, and using a tighter weave will also shift the fiber weave resonances to higher frequencies, and also reduce skew.

A simple way to suppress emissions from cavities in your board is to use a grounded via picket fence around specific circuits and the edge of your board. Sizing the via diameter and spacing allows you to create a resonant image of the cavity resonance, which suppresses emission. The optimal via spacing is one-eighth the wavelength (in the dielectric) of the resonance you want to suppress. While this structure carries greater fabrication costs, it can mean the difference between passing and failing EMC tests.



*Effect created by placing a grounded via picket fence around important circuits and the edge of the board. This suppresses radiated EMI as an image current is induced in different planes/vias.*

No matter which design choices you make to suppress radiated EMI in your board, you can bring them into your stackup and layout with the powerful PCB design and analysis tools in Altium Designer®. This complete set of design tools is built on top of a unified rules-driven design engine, allowing you to verify functionality and manufacturability as you create your layout. You'll also have a complete set of tools for analyzing signal integrity and preparing deliverables for your manufacturer.